FILE: 10375USF.RTF

WAFER LEVEL TESTING AND BUMPING PROCESS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 92103361, filed February 19, 2003. THIS APPLICATION IS A DIVISIONAL OF CAL 10/447,520 FILED ON 05/28/2003, NOW U.S. PATENT 6,869,809.

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to a testing and packaging process. More particularly, the present invention relates to a wafer level testing and bumping process.

Description of Related Art

[0002] Following the rapid development of semiconductor fabrication techniques, advanced and precise semiconductor devices are now being produced to meet the increased demand in many electronic products. In general, for the fabrication of semiconductors and the subsequent package/test, a front stage fabrication process is carried out after the design of the integrated circuit (IC). The front stage fabrication process includes fabricating integrated circuits on a wafer followed by testing the circuits. After sawing the wafer into individual chips, a wire bonding or a flip-chip bonding process is usually carried out to connect bonding pads on the active surface of the chip with contact pads on a carrier. The carrier is a substrate or a lead frame, for example. Using a flip-chip package as an example, a plurality of bonding pads is formed on the active surface of the chip prior to attaching a bump to each bonding pad.